Clean copy of claims amended herein.

B2

12. (Twice Amended) A delay circuit according to claim 2, wherein the MOS capacitor is a node disposed on a transmission path of a logic signal, and is at least represented by a single p-MOS transistor whose gate is connected to a first node of the inverter chain that changes a logic level of the logic signal from a high level to a low level, and whose source and drain are fixed at a power potential.